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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,474	05/07/2004	Ryoichi Watanabe	JP920030057US1	3473

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IBM MICROELECTRONICS
INTELLECTUAL PROPERTY LAW
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ESSEX JUNCTION, VT 05452

EXAMINER

VAN, LUAN V

ART UNIT	PAPER NUMBER
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1753

DATE MAILED: 04/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/709,474

Applicant(s)

WATANABE ET AL.

Examiner

Luan V. Van

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 07 May 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-9 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-9 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☒ None of:
- 1) ☒ Certified copies of the priority documents have been received.
 - 2) ☐ Certified copies of the priority documents have been received in Application No. _____.
 - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 07 May 2004.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claims 4-9 are objected to because of the following informalities:

The claims are missing the claim numbers.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over McPherson et al. in view of Miracky et al.

Regarding claim 1, McPherson et al. teach a method of forming a printed circuit board, the method comprising the steps of: the providing a substrate comprising a seed

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layer 11 (Fig. 1) formed by electroless plating (column 3 lines 24-27); forming a masking layer 13 on said seed layer to provide first regions of exposed seed layer; forming a circuit pattern 15 on said first regions of exposed seed layer by electrolytic plating (column 3 lines 57-60); removing said masking layer to expose second regions of said seed layer (column 4 lines 3-4); and etching said exposed second regions of said seed layer with an etching liquid (column 3 lines 29-31).

McPherson et al. differ from the instant claim in that the reference does not explicitly disclose the flash etch temperature.

However, it is conventionally known in the art that a metal etch rate is proportional to the temperature. Miracky et al., for example, teach a "process for laser-assisted liquid phase etching of copper conductors which includes the use of a solution of sulfuric acid and hydrogen peroxide in contact with an integrated circuit substrate and the provision of a laser beam to select substrate areas having copper conductors to be etched" (see abstract). Miracky et al. further disclose that "chemical-etching conditions, especially temperature, as established in the workcell such that without laser irradiation, etching takes place slowly, if at all. It is desirable that the solution be held at a relatively low temperature, e.g., in the range between about -5°C and 5°C, preferably at or below about 0°C. For example, the background etch rate for the 2%/1% solution is 1.1 um/hr at 0°C. (see Table I)" (column 4 lines 61-69).

Addressing claims 1 and 2, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified the method of McPherson et al. by etching copper at the temperature range of Miracky et al., because

etching in the temperature range of Miracky et al. reduces the copper etch rate, thus minimizing the undesirable etching of the copper conductors.

Regarding claim 3, McPherson et al. teach the masking layer comprises photoresist (column 3 lines 34-35).

Regarding claim 4, McPherson et al. teach wherein said seed layer and said circuit pattern comprise copper (column 3 lines 57-60 and column 4 lines 55-57).

Regarding claim 5, McPherson et al. suggest that their process is suitable for constructing circuit lines and pins having uniform cross-section at a wide range of sizes that are less than 0.030 inches (column 2 lines 5-35). Miracky et al. disclose that a multichip substrate for integrated circuits typically have widths of 1-30 μm (column 2 lines 9-13). It would have been obvious to one having ordinary skill in the art at the time the invention was made to have formed the circuit pattern of McPherson et al. such that the distance between the confronting portions is proportional to the dimensions of the circuit lines, because it would enable the fabrication of a high density circuit device.

Regarding claim 6, McPherson et al. teach the seed layer and the circuit pattern are formed by copper plating (column 3 lines 57-60 and column 4 lines 55-59).

Regarding claim 7-8, McPherson et al. is silent to the composition of the flash etching liquid, suggesting that the etchant for copper is conventionally known. Miracky et al. teach the copper is etched in sulfuric acid and hydrogen peroxide (column 5 lines 29-48). It would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified the method of McPherson et al. by using the etchant solution of Miracky et al., because the etch rate of copper in sulfuric

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acid/hydrogen peroxide is strongly dependent on temperature and thus the rate can be advantageously controlled (column 5 lines 15-20).

Regarding claim 9, the substrate is inherently dipped in an etching liquid, since the flash etch is performed in a liquid etched solution.

Conclusion

The prior art made of record and not relied upon is considered pertinent to the applicant's disclosure. Jones et al. further teach the etch rate/temperature dependence and the advantage of sulfuric acid/hydrogen peroxide copper etchant. Pace also teaches that copper etchants are used at temperatures between 15-50° C (column 7 lines 63-65). Needham and Gulla teach etching the seed layer.

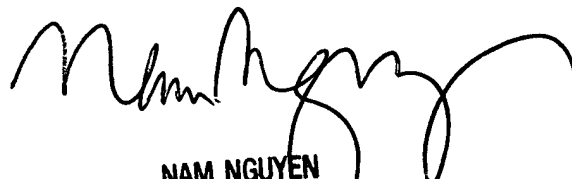
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luan V. Van whose telephone number is 571-272-8521. The examiner can normally be reached on M-F 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nam Nguyen can be reached on 571-272-1342. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LWV
April 17, 2006



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SUPERVISORY PATENT EXAMINER
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